TEXAS INSTRUMENTS

Linear Circuits

Operational Amplifier Macromodels

Errata

1990 Linear Products

Errata
Operational Amplifier Macromodels
Linear Circuits
Data Manual
1990

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introduction

Texas Instruments *Linear Circuits Operational Amplifier Macromodels Data Manual* (1990), distributed to thousands of users, has received highly favorable responses for the usefulness and accuracy of these models. However, some areas of concern have been identified and certain other considerations voiced as indicated in this errata. Future editions have been planned to address these concerns as well as include enhanced models for all new and advanced devices. As always, we consider your feedback an invaluable resource and appreciate your response.

These identified concerns can be categorized into two groups. The first concern is system/software matters and the second is device model anomalies.

system/software

If your system fails to run the simulation, possibly generating some obscure error code, it could be due to:

Embedded tabs: The text editor that generated the macromodels uses tabs for indentation. However, some simulators do not accept the TAB character (ASCII 9). In this case, the tabs can be stripped from the file using the short BASIC program shown below (Figure 1). As indentation is used only for readability, removing the tabs does not adversely affect the models' performance.

```
10      REM************************************************************
20      REM*** Tab-Stripping and Case-Conversion Program ************
30      REM*** Removes tabs and changes text to upper-case **********
40      REM************************************************************
50      KEY OFF: CLS
60      PRINT "Enter a filename to be converted..."
70      PRINT "Example:  C:\SPICE\TEST.TXT"
80      INPUT;SOURCE$
90      OPEN "I",#1,SOURCE$
100     CLS
110     PRINT "Enter a filename for the new converted file..."
120     INPUT;NUFLE$
130     OPEN "O",#2,NUFLE$:CNT = 0
140     WHILE NOT EOF(1)
150     CH$=INPUT$(1,#1)
160     IF CH$ = CHR$(9) THEN PRINT #2," ";:CNT = CNT+1:GOTO 190
170     IF (ASC(CH$) => 97 AND ASC(CH$) <= 122) THEN CDE = ASC(CH$)-
32:PRINT #2,CHR$(CDE);:GOTO 190
180     PRINT #2,CH$;
190     WEND
200     CLOSE
210     CLS:PRINT CNT;"tabs found and corrected."
220     PRINT "De-tabbed file is stored in "+CHR$(34)+NUFLE$+CHR$(34)
230     END
```

NOTE: Line 170 is word wrapped.

Figure 1. Tab-Stripping and Case-Conversion Program

Case sensitivity: Some versions of simulation software are case-sensitive, usually requiring all upper case characters. The macromodel text is lower case. The program in Figure 1 converts all text to upper case, thereby eliminating case disparities.

Negative resistances: On certain devices, the *PSpice® Parts™* software (used to construct the macromodels) generates negative resistance values for the re1 and re2 terms. Some simulators cannot handle negative resistances. This can be overcome by changing the "r" terms to "G"-type ideal generators using any text editor. The models affected and the corrected symbols are listed in Table 1.

Table 1. Macromodels Replacement for Negative Resistance

DEVICE TYPE	MACROMODEL PAGE NO.	ORIGINAL STATEMENT	REPLACEMENT STATEMENT
LM308	3-13	re1 13 10 -460.3 re2 14 10 -460.3	GE1 13 10 (10,13) 2.172E-3 GE2 14 10 (10,14) 2.172E-3
LT1001	3-18	re1 13 10 -532.7 re2 14 10 -532.7	GE1 13 10 (10,13) 1.877E-3 GE2 14 10 (10,14) 1.877E-3
LT1007	3-19	re1 13 10 -53.24 re2 14 10 -53.24	GE1 13 10 (10,13) 18.783E-3 GE2 14 10 (10,14) 18.783E-3
LT1012	3-21	re1 13 10 -460.6 re2 14 10 -460.6	GE1 13 10 (10,13) 2.171E-3 GE2 14 10 (10,14) 2.171E-3
LT1028	3-23	re1 13 10 -44.22 re2 14 10 -44.22	GE1 13 10 (10,13) 22.614E-3 GE2 14 10 (10,14) 22.614E-3
LT1037	3-24	re1 13 10 -66.35 re2 14 10 -66.35	GE1 13 10 (10,13) 15.072E-3 GE2 14 10 (10,14) 15.072E-3
TLE2022	3-100	re1 13 10 -31.95 re2 14 10 -31.95	GE1 13 10 (10,13) 31.299E-3 GE2 14 10 (10,14) 31.299E-3
TLE2024	3-101	re1 13 10 -31.90 re2 14 10 -31.90	GE1 13 10 (10,13) 31.348E-3 GE2 14 10 (10,14) 31.348E-3

device model anomalies

For no apparent reason simulations sometimes yield results that seem wrong. One probable cause is an invalid macromodel:

Supply voltages: The macromodels included in the first edition are modeled at only one set of supply voltages. Simulations run using other supply voltages could yield results that do not meet the accuracy guidelines. A new model must be generated for use with other supply values. For example, the TL031 is specified at ±15 V and ±5 V, but the model is only accurate at ±15 V. If simulated at ±5 V, the results do not correlate to the data sheet specifications. Table 2 lists all device types currently in the Macromodels Data Manual, their specified supply voltages, and the voltages used in creating the macromodels. Future additions are to include macromodels for each supply voltage specified in the data sheet.

Table 2. Macromodel Supply Voltage Considerations (continued)

DEVICE TYPE	SUPPLY VOLTAGE IN DATA SHEET (V)	SUPPLY VOLTAGE USED FOR MACROMODEL (V)	MACROMODEL DATA MANUAL PAGE NO.
TLC27L9	10, 5	10	3-89
TLC27M2	10, 5	10	3-90
TLC27M4	10, 5	10	3-91
TLC27M7	10, 5	10	3-92
TLC27M9	10, 5	10	3-93
TLC1078	10, 5	10	3-94
TLC1079	10, 5	10	3-95
TLC2201	± 5, 5	± 5	19†
TLC2652	± 5	± 5	20†
TLC2654	± 5	± 5	21†
TLE2021	± 15, 5	± 15	3-99
TLE2022	± 15, 5	± 15	3-100
TLE2024	± 15, 5	± 15	3-101
TLE2061	± 20, ± 15, ± 5	± 15	3-102
TLE2062	± 20, ± 15, ± 5	± 15	3-103
TLE2064	± 20, ± 15, ± 5	± 15	3-104
TLE2161	± 20, ± 15, ± 5	± 15	3-105
UA741	± 15	± 15	3-106
UA747	± 15	± 15	3-107
UA748	± 15	± 15	3-108

†The original macromodel has been entirely replaced by the macromodel in this errata.

Input Bias Currents: Simulation of devices having extremely low input bias currents (in the pA range) often generates abnormally high values for this parameter. This occurs primarily in CMOS products. Again, new models are needed to correct simulation errors. The macromodels known to exhibit this problem are listed in Table 3. Corrected macromodels are included in this errata on the pages shown.

Table 3. Macromodels with Input Bias Error

DEVICE TYPE	DATA MANUAL PAGE NO.	ERRATA PAGE NO.
ICL7652	3-3	7
LTC1052	3-25	8
TL136	3-65	9
TLC251C (H)	3-70	10
TLC252C	3-73	11
TLC254C	3-74	12
TLC271C (H)	3-79	13
TLC271C (M)	3-81	14
TLC272	3-82	15
TLC274	3-83	16
TLC277	3-84	17
TLC279	3-85	18
TLC2201	3-96	19
TLC2652	3-97	20
TLC2654	3-98	21

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SUPPLY VOLTAGE CONDITIONS: ±5 V

- Extremely Low Offset Voltage ... 5 μV Max
- Extremely Low Change In Offset Voltage with Temperature ... 0.003 μV/°C Typ
- Low Input Offset Current ... 30 pA Max
- A_{VD} ... 120 dB Min
- CMRR and k_{SVR} ... 110 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation with External Capacitors Connected to V_{DD-}

macromodel – applies to ICL7652, LTC7652

```
.SUBCKT ICL7652  1 2 3 4 5
*
  C1   11 12 3.804E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.342E9 -2E9 2E9 2E9 -2E9
  GA    6  0 11 12 125.7E-6
  GCM   0  6 10 99 25E-12
  ISS   3 10 DC 56.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 7.958E3
  RD2   4 12 7.958E3
  RO1   8  5 165
  RO2   7 99 165
  RP    3  4 6.667E3
  RSS  10 99 3.571E6
  VB    9  0 DC 0
  VC    3 53 DC .9
  VE   54  4 DC .8
  VLIM  7  8 DC 0
  VLP  91  0 DC 3.100
  VLN   0 92 DC 3.100
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=564.0E-6 VTO=-.19)
.ENDS
```

SUPPLY VOLTAGE CONDITIONS: ±5 V

- Input Offset Voltage ... 5 μV Max at 25°C
- Temperature Coefficient of Input Offset Voltage ... 0.01 μV/°C Typ
- Long-Term Drift of Input Offset Voltage 100 nV/mo Typ
- Input Bias Current ... 30 pA Max at 25°C
- Differential Voltage Amplification Over Full Temperature Range ... 120 dB Min
- Common-Mode Rejection Ratio Over Full Temperature Range ... 120 dB Min
- Supply Voltage Rejection Ratio Over Full Temperature Range ... 120 dB Min
- Single-Supply Operation from 4.75 V to 16 V (Input Voltage Range Extends to Ground)
- External Capacitors Can Be Returned to V_{DD-} with No Noise Degradation

macromodel – applies to LTC1052, LTC7652

```
.SUBCKT LTC1052  1 2 3 4 5
*
  C1   11 12 3.804E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.342E9 -2E9 2E9 2E9 -2E9
  GA    6  0 11 12 125.7E-6
  GCM   0  6 10 99 25E-12
  ISS   3 10 DC 56.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 7.958E3
  RD2   4 12 7.958E3
  RO1   8  5 165
  RO2   7 99 165
  RP    3  4 6.667E3
  RSS  10 99 3.571E6
  VB    9  0 DC 0
  VC    3 53 DC .9
  VE   54  4 DC .8
  VLIM  7  8 DC 0
  VLP  91  0 DC 3.100
  VLN   0 92 DC 3.100
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=564.0E-6 VTO=-.19)
.ENDS
```


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Table 2. Macromodel Supply Voltage Considerations

DEVICE TYPE	SUPPLY VOLTAGE IN DATA SHEET (V)	SUPPLY VOLTAGE USED FOR MACROMODEL (V)	MACROMODEL DATA MANUAL PAGE NO.
ICL7652	± 5	± 5	7†
LF347	± 15	± 15	3-4
LF351	± 15	± 15	3-5
LF353	± 15	± 15	3-6
LF411C	± 15	± 15	3-7
LF412C	± 15	± 15	3-8
LM101A	± 15	± 15	3-9
LM107	± 15	± 15	3-10
LM301A	± 15	± 15	3-11
LM307	± 15	± 15	3-12
LM308	± 15	± 15	3-13
LM318	± 15	± 15	3-14
LM324	± 5	± 5	3-15
LM348	± 15	± 15	3-16
LM358	± 5	± 5	3-17
LT1001	± 15	± 15	3-18
LT1007	± 15	± 15	3-19
LT1008	± 15	± 15	3-20
LT1012	± 15	± 15	3-21
LT1013	± 15, 5	± 15	3-22
LT1028	± 15	± 15	3-23
LT1037	± 15	± 15	3-24
LTC1052	± 5	± 5	8†
MC1458	± 15	± 15	3-26
MC3403	± 15, 5	± 15	3-27
NE5534	± 15	± 15	3-28
OP-07C	± 15	± 15	3-29
OP-07D	± 15	± 15	3-30
OP-07E	± 15	± 15	3-31
OP-27C	± 15	± 15	3-32
OP-27E	± 15	± 15	3-33
OP-27G	± 15	± 15	3-34
OP-37A	± 15	± 15	3-35
RC4136	± 15	± 15	3-36
RC4558	± 15	± 15	3-37
RC4559	± 15	± 15	3-38
TL022C	± 15	± 15	3-39
TL031	± 15, ± 5	± 15	3-40
TL032	± 15, ± 5	± 15	3-41
TL034	± 15, ± 5	± 15	3-42
TL044C	± 15	± 15	3-43
TL051	± 15, ± 5	± 15	3-44
TL052	± 15, ± 5	± 15	3-45

†The original macromodel has been entirely replaced by the macromodel in this errata.

Table 2. Macromodel Supply Voltage Considerations (continued)

DEVICE TYPE	SUPPLY VOLTAGE IN DATA SHEET (V)	SUPPLY VOLTAGE USED FOR MACROMODEL (V)	MACROMODEL DATA MANUAL PAGE NO.
TL054	± 15, ± 5	± 15	3-46
TL060	± 15	± 15	3-47
TL061	± 15	± 15	3-48
TL062	± 15	± 15	3-49
TL064	± 15	± 15	3-50
TL066C	± 15	± 15	3-51
TL070	± 15	± 15	3-52
TL071	± 15	± 15	3-53
TL072	± 15	± 15	3-54
TL074	± 15	± 15	3-55
TL075	± 15	± 15	3-56
TL080	± 15	± 15	3-57
TL081	± 15	± 15	3-58
TL082	± 15	± 15	3-59
TL083	± 15	± 15	3-60
TL084	± 15	± 15	3-61
TL085	± 15	± 15	3-62
TL087	± 15	± 15	3-63
TL088	± 15	± 15	3-64
TL136C	± 15	± 15	9†
TL287	± 15	± 15	3-66
TL288	± 15	± 15	3-67
TL321C	± 15	± 15	3-68
TL322C	± 15, 5	± 15	3-69
TLC251C (H)	10, 1.4	10	10†
TLC251C (L)	10, 1.4	10	3-71
TLC251C (M)	10, 1.4	10	3-72
TLC252C	10, 1.4	10	11†
TLC254C	10, 1.4	10	12†
TLC25L2C	10, 1.4	10	3-75
TLC25L4C	10, 1.4	10	3-76
TLC25M2C	10, 1.4	10	3-77
TLC25M4C	10, 1.4	10	3-78
TLC271C (H)	10, 5	10	13†
TLC271C (L)	10, 5	10	3-80
TLC271C (M)	10, 5	10	14†
TLC272	10, 5	10	15†
TLC274	10, 5	10	16†
TLC277	10, 5	10	17†
TLC279	10, 5	10	18†
TLC27L2	10, 5	10	3-86
TLC27L4	10, 5	10	3-87
TLC27L7	10, 5	10	3-88

†The original macromodel has been entirely replaced by the macromodel in this errata.

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SUPPLY VOLTAGE CONDITIONS: ±15 V

- Continuous-Short Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth . . . 3 MHz Typ
- Gain and Phase Match Between Amplifiers

macromodel – applies to TL136C

```
.SUBCKT TL136    1 2 3 4 5
*
  C1   11 12 3.460E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 6.96E6 -4E6 4E6 4E6 -4E6
  GA    6  0 11 12 377.0E-6
  GCM   0  6 10 99 11.92E-9
  IEE   3 10 DC 40.08E-6
  HLIM 90  0 VLIM 1K
  Q1   11  2 13 QX
  Q2   12  1 14 QX
  R2    6  9 100.0E3
  RC1   4 11 2.653E3
  RC2   4 12 2.653E3
  RE1  13 10 1.357E3
  RE2  14 10 1.357E3
  REE  10 99 4.990E6
  RO1   8  5 125
  RO2   7 99 125
  RP    3  4 24.79E3
  VB    9  0 DC 0
  VC    3 53 DC 2.700
  VE   54  4 DC 2.700
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL QX PNP(IS=800.0E-18 BF=500)
.ENDS
```

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SUPPLY VOLTAGE CONDITIONS: 10 V

- Wide Range of Supply Voltages 1.4 V to 16 V
- Common-Mode Input Voltage Range Includes the Negative Rail
- True Single-Supply Operation
- Low Noise . . . 30 nV/√Hz Typ at 1 kHz

macromodel – applies to TLC251, TLC251A, TLC251B

```
.SUBCKT TLC251H  1 2 3 4 5
*
  C1   11 12 2.591E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.635E6 -4E6 4E6 4E6 -4E6
  GA    6  0 11 12 163.4E-6
  GCM   0  6 10 99 13.04E-9
  ISS   3 10 DC 90.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 6.121E3
  RD2   4 12 6.121E3
  RO1   8  5 250
  RO2   7 99 75
  RP    3  4 10.00E3
  RSS  10 99 2.222E6
  VB    9  0 DC 0
  VC    3 53 DC 1.400
  VE   54  4 DC 1.400
  VLIM  7  8 DC 0
  VLP  91  0 DC 15
  VLN   0 92 DC 15
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=593.1E-6 VTO=-.219)
.ENDS
```


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SUPPLY VOLTAGE CONDITIONS: 10 V

- A-Suffix Versions Offer 5-mV V_{IO}
- B-Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 25 nV/$\sqrt{Hz}$ Typ at f = 1 kHz

macromodel – applies to TLC252, TLC252A, TLC252B

```
.SUBCKT TLC252C  1 2 3 4 5
*
  C1   11 12 2.591E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.635E6 -4E6 4E6 4E6 -4E6
  GA    6  0 11 12 163.4E-6
  GCM   0  6 10 99 13.04E-9
  ISS   3 10 DC 90.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 6.121E3
  RD2   4 12 6.121E3
  RO1   8  5 250
  RO2   7 99 75
  RP    3  4 10.00E3
  RSS  10 99 2.222E6
  VB    9  0 DC 0
  VC    3 53 DC 1.400
  VE   54  4 DC 1.400
  VLIM  7  8 DC 0
  VLP  91  0 DC 15
  VLN   0 92 DC 15
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=593.1E-6 VTO=-.219)
```

SUPPLY VOLTAGE CONDITIONS: 10 V

- A-Suffix Versions Offer 5-mV V_{IO}
- B-Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise ... 25 nV/$\sqrt{Hz}$ Typ at f = 1 kHz

macromodel – applies to TLC254, TLC254A, TLC254B

```
.SUBCKT TLC254C  1 2 3 4 5
*
  C1   11 12 2.591E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.635E6 -4E6 4E6 4E6 -4E6
  GA    6  0 11 12 163.4E-6
  GCM   0  6 10 99 13.04E-9
  ISS   3 10 DC 90.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 6.121E3
  RD2   4 12 6.121E3
  RO1   8  5 250
  RO2   7 99 75
  RP    3  4 10.00E3
  RSS  10 99 2.222E6
  VB    9  0 DC 0
  VC    3 53 DC 1.400
  VE   54  4 DC 1.400
  VLIM  7  8 DC 0
  VLP  91  0 DC 15
  VLN   0 92 DC 15
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=593.1E-6 VTO=-.219)
.ENDS
```

SUPPLY VOLTAGE CONDITIONS: 10 V

- Input Offset Voltage Drift ... 0.1 μV/moTyp, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  - −55°C to 125°C ... 5 V to 16 V
  - −40°C to 85°C ... 4 V to 16 V
  - 0°C to 70°C ... 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Low Noise ... 25 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10^{12} Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

macromodel – applies to TLC271, TLC271A, TLC271B

```
.SUBCKT TLC271H  1 2 3 4 5
*
  C1   11 12 4.693E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.354E6 -3E6 3E6 3E6 -3E6
  GA    6  0 11 12 175.9E-6
  GCM   0  6 10 99 19.786E-9
  ISS   3 10 DC 92.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 5.684E3
  RD2   4 12 5.684E3
  RO1   8  5 75
  RO2   7 99 75
  RP    3  4 10.53E3
  RSS  10 99 2.174E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC .7
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=350.0E-15 BETA=672.8E-6 VTO=-.195)
.ENDS
```

SUPPLY VOLTAGE CONDITIONS: 10 V

- Input Offset Voltage Drift ... 0.1 μV/moTyp, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  - −55°C to 125°C ... 5 V to 16 V
  - −40°C to 85°C ... 4 V to 16 V
  - 0°C to 70°C ... 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Low Noise ... 32 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10^{12} Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available In Tape and Reel
- Designed-In Latch-Up Immunity

macromodel – applies to TLC271, TLC271A, TLC271B

```
.SUBCKT TLC271M  1 2 3 4 5
*
  C1   11 12 6.62E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 33.77E6 -90E6 90E6 90E6 -90E6
  GA    6  0 11 12 54.66E-6
  GCM   0  6 10 99 2.181E-9
  ISS   3 10 DC 11.20E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 18.29E3
  RD2   4 12 18.29E3
  RO1   8  5 75
  RO2   7 99 75
  RP    3  4 69.9E3
  RSS  10 99 17.86E6
  VB    9  0 DC 0
  VC    3 53 DC 2
  VE   54  4 DC .7
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=350.0E-15 BETA=533.6E-6 VTO=-.035)
.ENDS
```


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SUPPLY VOLTAGE CONDITIONS: 10 V

- **Input Offset Voltage:**
  TLC272B ... 2 mV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift ... 0.1 μV/mo Typ, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C ... 4 V to 16 V
  −40°C to 85°C ... 4 V to 16 V
  0°C to 70°C ... 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise ... 25 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance ... 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

macromodel – applies to TLC272, TLC272A, TLC272B

```
.SUBCKT TLC272   1 2 3 4 5
*
  C1   11 12 4.693E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.354E6 -3E6 3E6 3E6 -3E6
  GA    6  0 11 12 175.9E-6
  GCM   0  6 10 99 19.786E-9
  ISS   3 10 DC 92.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 5.684E3
  RD2   4 12 5.684E3
  RO1   8  5 75
  RO2   7 99 75
  RP    3  4 10.53E3
  RSS  10 99 2.174E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC .7
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=350.0E-15 BETA=672.8E-6 VTO=-.195)
.ENDS
```

JANUARY 1990 – REVISED JULY 1990

SUPPLY VOLTAGE CONDITIONS: 10 V

- Input Offset Voltage:
  TLC274B ... 2 mV Max at 25°C,
  V_{DD} = 5 V
- Input Offset Voltage Drift ... 0.1 μV/mo Typ, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  −55°C to 125°C ... 4 V to 16 V
  −40°C to 85°C ... 4 V to 16 V
  0°C to 70°C ... 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Low Noise ... 25 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10^{12} Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

macromodel – applies to TLC274, TLC274A, TLC274B

```
.SUBCKT TLC274   1 2 3 4 5
*
  C1   11 12 4.693E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.354E6 -3E6 3E6 3E6 -3E6
  GA    6  0 11 12 175.9E-6
  GCM   0  6 10 99 19.786E-9
  ISS   3 10 DC 92.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 5.684E3
  RD2   4 12 5.684E3
  RO1   8  5 75
  RO2   7 99 75
  RP    3  4 10.53E3
  RSS  10 99 2.174E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC .7
  VLIM  7  8 DC 0
  VLP  91  0 DC 25
  VLN   0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=350.0E-15 BETA=672.8E-6 VTO=-.195)
.ENDS
```


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SUPPLY VOLTAGE CONDITIONS: 10 V

- Trimmed Offset Voltage ... 500 μV Max at 25°C, V_{DD} = 5 V
- Input Offset Voltage Drift ... 0.1 μV/mo Typ, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  - −55°C to 125°C ... 4 V to 16 V
  - −40°C to 85°C ... 4 V to 16 V
  - 0°C to 70°C ... 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Low Noise ... 25 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10^{12} Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

macromodel – applies to TLC277

```
.SUBCKT TLC277   1 2 3 4 5
*
  C1   11 12 4.693E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.221E6 -3E6 3E6 3E6 -3E6
  GA    6  0 11 12 175.9E-6
  GCM   0  6 10 99 19.786E-9
  ISS   3 10 DC 92.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 5.684E3
  RD2   4 12 5.684E3
  RO1   8  5 85
  RO2   7 99 85
  RP    3  4 10.53E3
  RSS  10 99 2.174E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC .7
  VLIM  7  8 DC 0
  VLP  91  0 DC 20
  VLN   0 92 DC 20
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=350.0E-15 BETA=672.8E-6 VTO=-.19)
.ENDS
```

SUPPLY VOLTAGE CONDITIONS: 10 V

- Trimmed Offset Voltage ... 900 μV Max at 25°C, V_{DD} = 5 V
- Input Offset Voltage Drift ... 0.1 μV/mo Typ, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  - −55°C to 125°C ... 4 V to 16 V
  - −40°C to 85°C ... 4 V to 16 V
  - 0°C to 70°C ... 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Low Noise ... 25 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10^{12} Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

macromodel – applies to TLC279

```
.SUBCKT TLC279   1 2 3 4 5
*
  C1   11 12 4.693E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.221E6 -3E6 3E6 3E6 -3E6
  GA    6  0 11 12 175.9E-6
  GCM   0  6 10 99 19.786E-9
  ISS   3 10 DC 92.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 5.684E3
  RD2   4 12 5.684E3
  RO1   8  5 85
  RO2   7 99 85
  RP    3  4 10.53E3
  RSS  10 99 2.174E6
  VB    9  0 DC 0
  VC    3 53 DC 2.200
  VE   54  4 DC .7
  VLIM  7  8 DC 0
  VLP  91  0 DC 20
  VLN   0 92 DC 20
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=350.0E-15 BETA=672.8E-6 VTO=-.19)
.ENDS
```


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SUPPLY VOLTAGE CONDITIONS: ±5 V

- TLC2201B Is 100% Tested for Noise:
  25 nV/√Hz Max at f = 10 Hz
  12 nV/√Hz Max at f = 1 kHz
- Low Input Offset Voltage ... 200 μV Max
- Excellent Offset Voltage Stability with Temperature ... 0.5 μV/°C Typ
- Low Input Bias Current ... 1 pA Typ at T_A = 25°C
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail

macromodel – applies to TLC2201, TLC2201A, TLC2201B

```
.SUBCKT TLC2201  1 2 3 4 5
*
  C1   11 12 4.004E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 2.440E6 -2E6 2E6 2E6 -2E6
  GA    6  0 11 12 113.1E-6
  GCM   0  6 10 99 601.1E-12
  ISS   3 10 DC 54.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 8.842E3
  RD2   4 12 8.842E3
  RO1   8  5 188
  RO2   7 99 187
  RP    3  4 9.091E3
  RSS  10 99 3.704E6
  VB    9  0 DC 0
  VC    3 53 DC .9
  VE   54  4 DC .8
  VLIM  7  8 DC 0
  VLP  91  0 DC 3
  VLN   0 92 DC 3
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=473.7E-6 VTO=-.18)
.ENDS
```

JANUARY 1990 – REVISED JULY 1990

SUPPLY VOLTAGE CONDITIONS: ±5 V

- Extremely Low Offset Voltage ... 1 μV Max
- Extremely Low Change in Offset Voltage with Temperature ... 0.003 μV/°C Typ
- Low Input Offset Current ... 500 pA Max at T_A = −55°C to 125°C
- A_{VD} ... 135 dB Min
- CMRR and k_{SVR} ... 120 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation with External Capacitors Connected to V_{DD-}

macromodel – applies to TLC2652, TLC2652A

```
.SUBCKT TLC2652  1 2 3 4 5
*
  C1   11 12 3.804E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.342E9 -2E9 2E9 2E9 -2E9
  GA    6  0 11 12 125.7E-6
  GCM   0  6 10 99 25E-12
  ISS   3 10 DC 56.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 7.958E3
  RD2   4 12 7.958E3
  RO1   8  5 165
  RO2   7 99 165
  RP    3  4 6.667E3
  RSS  10 99 3.571E6
  VB    9  0 DC 0
  VC    3 53 DC .9
  VE   54  4 DC .8
  VLIM  7  8 DC 0
  VLP  91  0 DC 3.100
  VLN   0 92 DC 3.100
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=564.0E-6 VTO=-.19)
.ENDS
```


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SUPPLY VOLTAGE CONDITIONS: ±5 V

- **Input Noise Voltage:**
  0.5 μV p-p Typ, f = 0 to 1 Hz
  1.5 μV p-p Typ, f = 0 to 10 Hz
  47 nV/√Hz Typ, f = 10 Hz
  13 nV/√Hz Typ, f = 1 kHz
- **High Chopping Frequency ... 10 kHz Typ**
- **No Clock Noise Below 10 kHz**
- **No Intermodulation Error Below 5 kHz**
- **Low Input Offset Voltage ... 10 μV Max**
- **Excellent Offset Voltage Stability with Temperature ... 0.3 μV/°C Max**
- **A_{VD} ... 135 dB Min**
- **CMRR ... 110 dB Min**
- **k_{SVR} ... 120 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation with External Capacitors Connected to V_{DD-}**

macromodel – applies to TLC2654, TLC2654A

```
.SUBCKT TLC2654  1 2 3 4 5
*
  C1   11 12 4.004E-12
  C2    6  7 20.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
  FB    7 99 POLY(5) VB VC VE VLP VLN 0 1.798E9 -1E9 1E9 1E9 -1E9
  GA    6  0 11 12 138.2E-6
  GCM   0  6 10 99 154.73E-12
  ISS   3 10 DC 40.00E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1   4 11 7.234E3
  RD2   4 12 7.234E3
  RO1   8  5 165
  RO2   7 99 165
  RP    3  4 6.667E3
  RSS  10 99 5.000E6
  VB    9  0 DC 0
  VC    3 53 DC .9
  VE   54  4 DC .8
  VLIM  7  8 DC 0
  VLP  91  0 DC 3.100
  VLN   0 92 DC 3.100
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=25.00E-12 BETA=955.4E-6 VTO=-1)
.ENDS
```

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